In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed or most recently amended.

Paragraph 0024:

As illustrated in Figure 1, a layer 150 is provided (in the case of copper but generally not in the case of aluminum or tungsten) over the M1 layer. This barrier layer is preferably an insulator of silicon nitride, silicon carbide or the like which can function as both a barrier, particularly when a low-k material that is particularly subject to diffusion of moisture is used as the ILD, and an etch stop for the subsequent via level and is sometimes referred to as a cap layer or (somewhat inaccurately) as a copper cap. The ILD layer 160 is then formed and patterned as both a barrier to copper out-diffusion and, particularly, to form the wiring trenches 170 and via openings 180 in accordance with the chip design. The cap layer provides substantial convenience as an etch stop in this process and then opened using the patterned ILD layer as a mask using a process well-understood in the art. Then, as shown in Figure 2, a layer or ~~fil~~ fill of alloying material 210 is applied, preferably by sputtering at high temperature, to form an alloy with exposed copper as it is deposited. A high temperature process is much preferred to assure that all alloying material deposited on exposed copper 130 is reacted with the copper as it is deposited, as illustrated at 220, so that no unreacted alloying material will remain at the trench bottom where it might be available to diffuse into and alloy with the copper at a later time.

Paragraph 0033:

Further, as shown in Figure 5, this anisotropic etch process also optionally but preferably recesses (415) the copper of conductor 120 at the trench bottom which increases the area of the copper to copper interface and provides for current to largely bypass the alloy annulus. A tantalum second barrier layer 420' (which may be required to protect the low-k ILD, if used) and a seed layer 430 are then applied as in the first embodiment and copper 440 is applied, preferably by plating (although other processes may allow omission of the seed layer, as is well-understood in the art) and planarized. The second embodiment of the invention is completed by annealing to form an alloy annulus 450 below the sidewalls 410 as shown in Figure 6 where the alloying material contacts the underlying copper, as limited by the barrier layer 420 (and 420'). A sectional view of the alloy annulus at section A-A is shown in Figure 6A. The annealing can be performed at any time after barrier layer 420 is in place and annealing prior to deposition of the via copper may be preferable in some circumstances.